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EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,811	NAGANO, KOUICHI	
	Examiner	Art Unit	
	Mohsin (Ben) Benghuzzi M.B.	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 16, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *July 31, 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *July 31, 2003* / July 14, 2005 / Feb. 13, 2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's argument with respect to the rejection of claim 11 under Kim, US 5,940,451, (see the fifth paragraph, Response to Rejection of Claim 1 and 11, page 3) has been considered and is persuasive. Therefore, the rejection has been withdrawn.

2. Applicant's arguments with respect to the rejection of claims 1 and 11 under Borazjani, US 5,719,867, have been fully considered but are moot in view of the new ground of rejection.

(1) Applicant's argument – {...Borazjani does not disclose, among other things, "a peak detection circuit for receiving a digitized wobble signal," recited in independent claim 1. The digitized wobble signal indicates "address information recorded on a DVD by phase modulation of a wobble signal" (see the preamble of claim 1).} (Second paragraph under **The Rejection of Claims 1-3, 9, 11, and 18**, page 4).

Examiner's response - Applicant's argument has been considered but is moot in view of the new ground of rejection. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani in view of Ueno. Borazjani discloses a peak detection circuit for receiving a signal and detecting a peak value (Column 22 Line 3 and Column 24 Lines 46-49, wherein, it is interpreted that 'further steps are taken for peak detection' is in reference to steps taken by the amplitude detector 408 in Fig. 9), and Ueno discloses a received signal that is a wobble signal representing address

information (Abstract, lines 1-3, paragraph 0014, lines 4-8, paragraph 0083, and paragraph 0084).

(2) Applicant's argument – {...Borazjani does not disclose, among other things, "a multiplier for receiving a digitized wobble signal and multiplying the wobble signal by the gain adjustment coefficient," recited in independent claim 11. The digitized wobble signal indicates "address information recorded on a DVD by phase modulation of a wobble signal" (see the preamble of claim 11).} (Fourth paragraph under **The Rejection of Claims 1-3, 9, 11, and 18**, page 4).

Examiner's response - Applicant's argument has been considered but is moot in view of the new ground of rejection. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani in view of Ueno. Borazjani discloses a multiplier for receiving a signal and multiplying the signal by the gain adjustment coefficient (406 in Fig. 9, Column 22 Lines 3-5, and Column 24 Lines 46-49, wherein, the multiplying factor M is interpreted as the gain adjustment coefficient), and, as discussed above, Ueno discloses a received signal that is a wobble signal representing address information (Abstract, lines 1-3, paragraph 0014, lines 4-8, paragraph 0083, and paragraph 0084).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 9, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani (US 5,719,867) in view of Ueno (US Pub 2003/0058764).

1) Regarding claim 1:

Borazjani discloses a digital AGC circuit comprising:

a peak detection circuit for receiving a signal and detecting a peak value (Column 22 Line 3 and Column 24 Lines 46-49, wherein, it is interpreted that 'further steps are taken for peak detection' is in reference to steps taken by the amplitude detector 408 in Fig. 9);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 22 lines 4-5 and Column 24 Lines 43-49 , wherein, the multiplying factor M is interpreted as the gain adjustment coefficient); and

a multiplier for multiplying the signal by the gain adjustment coefficient (406 in Fig. 9, Column 22 Lines 3-5, and Column 24 Lines 46-49).

Borazjani does not disclose the received signal to be a wobble signal, however, Ueno specifically discloses a received signal that is a wobble signal representing address information (Abstract, lines 1-3, paragraph 0014, lines 4-8, paragraph 0083, and paragraph 0084). Encoding address information on a DVD or CD surface using a wobble signal is well known in the relevant art. The advantage of encoding using a wobble signal is that a constant linear scanning velocity is maintained.

Regarding the peak value being detected in a time period equal to or more than a half period of the wobble signal, it is well know in the art that the detection of the peak of a sinusoidal signal, i.e., a wobble signal, must occur within at least a half period of the

sinusoidal signal, as a peak, either positive or negative, surely occurs within a half period of a sinusoidal signal.

Regarding the signal multiplied by the multiplier being a wobble signal, as discussed above in the claim, Ueno specifically discloses a received signal that is a wobble signal representing address information (Abstract, lines 1-3, paragraph 0014, lines 4-8, paragraph 0083, and paragraph 0084).

2) Regarding claim 2:

Borazjani discloses an AGC circuit further comprising a delay circuit for delaying the wobble signal and supplying the delayed signal to the multiplier (Column 6 Lines 15-17).

3) Regarding claim 3:

Borazjani discloses an AGC circuit further comprising a limiter for limiting the gain adjustment coefficient to be supplied from the gain computation circuit to the multiplier to within a fixed range (Column 24 Lines 44-45, wherein, shifter limits output to the range of 0.5 to 2 times its nominal input).

4) Regarding claim 9:

Borazjani discloses an AGC circuit wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit (Column 26 Lines 6-8 and 627 in Fig. 12, wherein, in determining the average, a divider is utilized).

5) Regarding claim 11:

Borazjani discloses a digital AGC circuit comprising:

a peak detection circuit for receiving a signal and detecting a peak value (Column 22 Line 3 and Column 24 Lines 46-49, wherein, it is interpreted that 'further steps are taken for peak detection' is in reference to steps taken by the amplitude detector 408 in Fig. 9);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 22 lines 4-5 and Column 24 Lines 43-49 , wherein, the multiplying factor M is interpreted as the adjustment coefficient); and

a multiplier for receiving a signal and multiplying the signal by the gain adjustment coefficient (406 in Fig. 9, Column 22 Lines 3-5, and Column 24 Lines 46-49).

Regarding the signal received by the peak detection circuit being the output of the digital AGC circuit, the output of the AGC is still a sinusoidal signal and, thus, virtually no different in signal characteristics from the input wobble signal and, as discussed in claim 1 above, Ueno specifically discloses a received signal that is a wobble signal representing address information (Abstract, lines 1-3, paragraph 0014, lines 4-8, paragraph 0083, and paragraph 0084).

Regarding the peak value being detected in a time period equal to or more than a half period of the input, as discussed in claim 1 above, it is well know in the art that the detection of the peak of a sinusoidal signal must occur within at least a half period of the sinusoidal signal.

6) Regarding claim 18:

Borazjani discloses an AGC circuit wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit (Column 26 Lines 6-8 and 627 in Fig. 12, wherein, in determining the average, a divider is utilized).

5. Claims 4-8, and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani (US 5,719,867) and Ueno (US Pub 2003/0058764), and further in view of Kiyanagi et al. (US 6,029,056).

1) Regarding claim 4:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14, wherein, when the count changes from 0 to 1 is interpreted as the counter counting one period).

It is advantageous to use a counter in the AGC of Borazjani. Channel clock cycles must be counted in order to determine elapsed time, and therefore, determine the needed wobble signal period. Using a counter will allow for the counting of clock cycles. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

2) Regarding claim 5:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an absolute value circuit for computing the absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit (Column 25 Lines 51-54).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period

counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

3) Regarding claim 6:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period

counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

4) Regarding claim 7:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit (Column 25 Lines 54-56, wherein, subtracting is interpreted as computing the difference).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, as discussed above in claim 4, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al.

teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

5) Regarding claim 8:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to the output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an adder for adding the detected positive peak value and negative peak value (Column 26 Line 62-63);

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani or Ueno do not disclose, a half-period counter for counting a half period of the wobble signal. As discussed in claim 4 above, Kiyanagi et al. discloses a one-period counter (Column 9 Lines 13-14), however, it is well known in the art that a half-period counter is similar in operation to a one-period counter. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to include a half-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal half-period.

6) Regarding claim 12:

Borazjani or Ueno do not disclose an AGC circuit further comprising an integrator for integrating the gain adjustment coefficient received from the gain computation circuit and supplying the result to the multiplier. However, Kiyanagi et al. discloses a circuit comprising an integrator for integrating the gain adjustment coefficient received from the gain computation circuit and supplying the result to the multiplier (Column 9 Lines 12-13). It is well known in the art that an integrator is used to smooth out a signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integrator, as Kiyanagi et al. teaches, in the circuit of Borazjani and Ueno in order to smooth out the gain adjustment coefficient signal received from the gain computation circuit.

7) Regarding claim 13:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit

(Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

8) Regarding claim 14:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an absolute value circuit for computing the absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit (Column 25 Lines 51-54).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

9) Regarding claim 15:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

10)Regarding claim 16:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit (Column 25 Lines 54-56, wherein, subtracting is interpreted as computing the difference).

Borazjani or Ueno do not disclose, a one-period counter for counting one period of the wobble signal. However, as discussed above in claim 4, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9

Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

11)Regarding claim 17:

Borazjani discloses an AGC circuit wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to an output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an adder for adding the detected positive peak value and negative peak value (Column 26 Line 62-63);

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani or Ueno do not disclose, a half-period counter for counting a half period of the wobble signal. As discussed in claim 4 above, Kiyanagi et al. discloses a one-

period counter (Column 9 Lines 13-14), however, it is well known in the art that a half-period counter is similar in operation to a one-period counter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a half-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani and Ueno in order to be able to count clock cycles, and therefore, be able to determine wobble signal half-period.

6. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani (US 5,719,867) and Ueno (US Pub 2003/0058764), and further in view of Tenca et al. (US 7,046,800).

1) Regarding claim 10:

Borazjani or Ueno do not disclose, wherein the divider is constructed of a bit shift circuit for performing bit shift division. However, Tenca et al. discloses, wherein the divider is constructed of a bit shift circuit for performing bit shift division (Column 2 Lines 18-20).

It is advantageous to employ bit-shift division. Bit-shift division is a simple operation and is easy to implement (See Tenca et al., Column 2 Lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use bit-shift division, as Tenca et al teaches, in the AGC of Borazjani and Ueno in order to simplify the division operation.

2) Regarding claim 19:

Borazjani or Ueno do not disclose, wherein the divider is constructed of a bit shift circuit for performing bit shift division. However, Tenca et al. discloses, wherein the divider is constructed of a bit shift circuit for performing bit shift division (Column 2 Lines 18-20).

Therefore, as discussed in claim 10 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use bit-shift division, as Tenca et al teaches, in the AGC of Borazjani and Ueno in order to simplify the division operation.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Haefner et al. (US 5,620,466) discloses a digital automatic gain control using separate gain control and threshold templating.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached on 8:30- 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi March 23, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER